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(54) PWM power amplifier with digital input

(57) A digital input PWM power amplifier comprises:

an oversampling and noise shaping circuit receiving pulse code modulated (PCM) digital input data organized in words of a first number M of bits at a certain bit rate (Fin) and outputting pulse code modulated digital data organized in words of a smaller number N of bits at a multiple bit rate (Fin*K);
a first bus transmitting a first number (P) of most significant bits (MSB) of said N bit words output from said first circuit and a second bus transmitting a second number (S) of least significant bits of said N bit words output from said first circuit;
first and second PCM/PWM converters, respectively fed with said first and second number of bits transmitted through said first and said second bus, each converter including a counter driven by a clock signal (Fclock) of frequency equal to the product of the bit rate (Fin*K) of the MSB and LSB bits transmitted on the respective bus and the square of the respective number of bits (P, S) generating reference digital words composed of said respective number of bits (P, S), defining ramps of digital values with a frequency identical to said multiple bit rate (Fin*K), and a digital comparator receiving through a first input said reference digital words and through a second input the respective first and second number of bits (MSB, LSB) and outputting a respective PWM signal (MSBdig, LSBdig);
the PWM signal (MSBig) output by said first converter, being summed to the so attenuated PWM signal (LSBdig) output by said second converter on the inverting input node (-) of said output power stage.

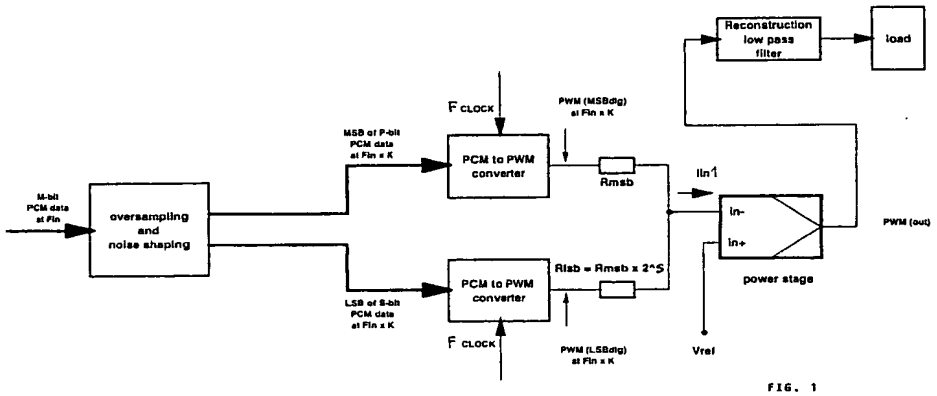

FIG. 1

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to high efficiency low frequency amplifiers, commonly referred to as class-D amplifiers and particularly though not exclusively to class-D audio amplifiers.

BACKGROUND OF THE INVENTION

[0002] The efforts for reducing energy consumption, weight and size of heat sinks of manufacturers of consumer apparatuses, for example in the field of car entertainment, have generated a demand for power amplifiers with a greater efficiency than the traditional class-AB amplifiers.

[0003] So-called class-D amplifiers have been proposed to respond to these requisites. Substantially, these amplifiers include a DC to AC converter circuit (DAC), which produces a PWM output signal. This PWM signal drives output power devices that through a passive lowpass filter for reconstructing an amplified analog (audio) signal drive a load (for example a speaker) that may be a part of the lowpass filter.

[0004] The analysis of the behavior of a single ended amplifier with an analog input and a PWM output (a class-D amplifier) is described in the paper "Analysis of a quality class-D amplifier", F. A. Himmelstoss, et al., I. E.E.E. Transactions on Consumer Electronics, Vol. 42, No. 3, August 1996.

[0005] On the other hand, the increasing interest in digital audio signal processing will make more convenient in many occasions to use digital amplifiers rather than analog amplifiers.

[0006] Presently, there are no known commercial applications of digital input amplifiers but few articles that describe possible design approaches:

- "Noise shaping and Pulse-Width Modulation for All-Digital Audio Power Amplifiers" by J.M. Goldberg and M.B. Sandler, Journal Audio Eng. Doc., Vol. 39, No. 6, 1991 June. This system described does not use any feedback circuit on the final stage, which to some extent penalizes the performance in terms of distortion and noise rejection. The performance appears to be strictly dependent on the characteristics of the components of the power stage (Fig. 8);
- "All digital Power Amplifier Based on Pulse Width Modulation" by M.S. Pedersen and M. Shajaan, presented during the 96th AES convention (Audio Engineering Society), 26th February, 1st March, 1994, in Amsterdam. According to this design approach there is no feedback circuit. The system appears to be burdened by resorting to a linearized PWM;
- "A Sigma-Delta Power Amplifier for Digital Input Signals" by Klugbauer-Heilmeier presented during the 102nd AES (Audio Engineering Society) convention 22nd-25th March, 1997, in Munich. The article describes a pulse density modulation (PDM) amplifier requiring a high switching frequency besides an antialiasing filter in the feedback path.

OBJECT AND SUMMARY OF THE INVENTION

[0007] The main objective of the present invention is to devise a digital input PWM power amplifier functioning at a relatively low switching frequency in order to achieve a high efficiency, being easy to make and having a low sensitivity to the spread of the actual values of the parameters of the circuit's components, and able to function at the lowest possible driving frequency of the PCM/PWM converter, without requiring integrated lowpass filters. The only filter of the system being a lowpass filter connected in cascade of the amplifier output, which is in any case always present in switching output stages.

[0008] These important objectives are effectively attained by the amplifier of the present invention.

[0009] Essentially, the PWM power amplifier of the invention comprises an oversampling and noise shaping block receiving PCM (Pulse Code Modulation) input digital data, organized in words composed of a certain number (M) of bits and outputting PCM digital data converted into words composed of a lower number (N) of bits than the number of bits of the input data (M>N) at a multiple bit rate (Fin*k) of the bit rate (Fin) of the input data.

[0010] A first bus transmits a first fraction (P) of most significant bits (MSB) of the words output from the first block and a second bus transmits the remaining (S) least significant bits (LSB) of the words output from said first block.

[0011] ach of the first and second PCM/PWM converters, fed with data transmitted on the first and on the second bus, respectively, is composed of a counter that is reset by the transitions of the digital value of data fed to the respective converter. The converter functions in an up/down mode and is fed with at least a clock signal (Fclock) whose frequency is equal to the multiplied bit rate (Fin*k) of the data transmitted on the respective bus of the converter multiplied by the square of the relative number of bits two (P or S) of the transmitted words and generate reference digital words composed by the respective number of bits (P or S), representing incremental and decremental digital values, defining single or multiple slope rising and descending ramps of digital values, whose rate is identical to the bit rate of the data fed to the converter. A digital comparator receives through a first input the reference digital words generated by the up-down counter and through a second input the input data and outputs a PWM digital signal (MSBdlg, LSBdig) at a switching frequency equal to the bit rte of the input digital data stream.

[0012] The PWM output signal (MSBdig) of the first

converter that receives the fraction (P) of most significant bits is summed on the inverting input node (-) of a final power amplifying stage of the amplifier to the PWM output signal (LSBdig) of the second converter (LSBdig), preventively attenuated by a ratio equivalent to the square of the number (S) of bits transmitted through the second bus to the input of the second converter.

[0013] The pair of PCM/PWM converters may be of the single or multiple ramp type.

[0014] The use of double ramp converters, that is with a succession of rising and falling ramps (that is a reference signal substantially of triangular waveform) enhances the amplifier performance in terms of distortion and of signal to noise ratio, compared to a single ramp converter (that is using a saw-tooth reference signal).

[0015] The output signal produced by the single final power stage in the case of a single ended amplifier or of the two final power stages in the case of a bridge configuration, that is, upstream of the lowpass analog signal reconstructing filter(s), is a PWM signal whose frequency is equal to the output signal (MSBdig) produced by the first converter but having a different duty-cycle in function of the following parameters:

a) supply voltage of the final power stage;
b) nonlinearity and losses of the final power stage;
c) correction made to the signal (LSBdig) output by the second converter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The various aspects and advantages of the invention will become even more evident through the following description of several embodiments and by referring to the annexed drawings, wherein:

Figure 1 is a block diagram of the basic structure of the PWM power amplifier of the invention, according to a first embodiment;
Figure 2 shows the internal structure of the final power stage;
Figure 3 shows the internal structure of each of the two PCM/PWM converters, according to a single ramp embodiment;
Figure 4 shows the operation waveforms of the PCM/PWM single ramp converter;
Figure 5 is a block diagram of the basic structure of the amplifier of the invention according to an alternative embodiment relative to the use of double ramp PCM/PWM converters;
Figure 6 shows the internal structure of the PCM/PWM double ramp converter;
Figure 7 shows the operation waveforms of the double ramp PCM/PWM converter;
Figure 8, 9, 10 and **11** show different embodiments of a bridge amplifier according to the present invention.

DESCRIPTION OF SEVERAL EMBODIMENTS OF THE INVENTION

[0017] By referring to the basic scheme of Fig. 1, each digital M bit word of the digital input data stream with a (Fin) bit rate, is converted by way of oversampling and noise shaping techniques into an N bit word of a lower number of bits than the input words (M>N) and with a multiple bit rate, Fin*k.

[0018] The N bits that compose the output words of the noise shaping and oversampling block are divided on two distinct buses. The first bus transmits a first fractional number P of most significant bits (MSB) while he second bus transmits the remaining number S of least significant bits (LSB).

[0019] The most significant bits (MSB) are sent to a first PCM/PWM converter whereas the S least significant bits (LSB) are sent to a second PCM/PWM converter.

[0020] The subdivision of the N bits into which the M bit PCM input digital data are reorganized permits to employ clock frequencies not excessively high when converting the PCM data to a PWM signal. Indeed, assuming a transformation into a PWM signal of a 16 bit PCM signal at 44.1 kHz without a detectable degradation of the signal/noise ratio, it would be necessary to use a sampling clock of $44100 \cdot 2^{16} = 2.8$GHz, which is substantially beyond the possibilities of implementation in present integrated circuits.

[0021] Another problem that is overcome by such subdivision is that the switching frequency of the output PWM signal, that for the example considered is 44.1 kHz, would be in any case too close to the maximum frequency to be played-back (generally of about 20kHz in an audio system), causing problems of harmonic distortion, of linearity and of signal residues with the PWM switching frequency downstream of the reconstructing lowpass filter.

[0022] Considering that the switching frequencies of PWM amplifiers are commonly comprised between 100Hz and 500kHz, and assuming a switching frequency of the PWM signal sufficiently far from the audio band, for example about $44100 \cdot 8 = 352.8$kHz, with a number P of MSB equal to 6 and the number S of LSB equal to 6, the clock frequency required by the PCM/PWM converters is $352800 \cdot 2^6 = 22.57$MHz, which may be easily handled with present fabrication techniques of integrated circuits.

[0023] Fig. 2 shows the internal structure that may be used to realize the final power amplifying block.

[0024] This class-D power amplifying module is described and illustrated in the European patent No. 98830685.8, filed on 13th November, 1998, in the name of the same applicant. The circuit does not require the generation of a reference triangular wave or any self-oscillating structures, making it usable also for analog inputs. Different inputs may be selected by a dedicated input configuration network (not shown as in the figure

it would be irrelevant in the present context).

[0025] Figures 3 and 4 show respectively the functional block diagram and the operation functioning waveforms of each PCM/PWM converter used in the amplifier scheme of Fig. 1, the signal indications being those of the first of the two converters fed through the P bit (MSB) bus.

[0026] According to this embodiment, both converters are of single ramp type. The ramp is generated by a cyclic and resettable up-counter, fed with a clock signal Fclock of a frequency equal to the product of the bit rate of the data transmitted on the respective bus and the square of the number of bit in which the fed data are organized.

[0027] The signal output from each of the two PCM/PWM converters is a PWM signal, whose duty cycle depends on the MSB or LSB input data.

[0028] By referring to the complete diagram of Fig. 1, the pair of PWM signals obtained from the separate conversion of the two portions of bits, respectively MSBdig and LSBdig, are eventually added on the inverting input node (-) of the final power amplifying module, after the LSBdig PWM signal is attenuated, by a factor equivalent to a ratio equivalent to the square of the number S of bits input through the second bus to the second converter.

[0029] In this way, the main PWM signal MSBdig, generated produced by the first PCM/PWM converter, drives by the output stage determining a switching frequency equal to Fin*K. On the other hand, the attenuated PWM signal LSBdig generated by the second converter PCM/PWM drives the output stage with a weight reduced by $1/2^S$ and thereby it does not affect the switching frequency of the output power stage but modulates the output PWM signal compensating for nonlinearities and attenuating the noise introduced by the quantization of a reduced number P of bits of the main PWM signal MSBdig.

[0030] An alternative embodiment of the amplifier of the invention is shown in Fig. 5. According to this embodiment, the use of double ramp PCM/PWM converters determines a frequency of their respective PWM output signals halved in respect to the bit rate of the input PCM data.

[0031] Figures 6 and 7 show respectively the functional block diagram of the two PCM/PWM double ramp converters and the relative operation waveforms. The indications refer to the first of the two converters, fed through the P bit bus (MSB).

[0032] Fig. 6 shows the feeding of a second clock signal Fup/down with the same multiplied frequency Fin*K of the data input to the converter that synchronizes the ramp inversions.

[0033] Of course the amplifier of the invention may also be realized in the form of a bridge amplifier by using two final power amplifying stages driven in phase opposition rather than in a single ended form.

[0034] By way of example, Fig. 8 shows the diagram of a bridge version of the amplifier, wherein the required inversion is implemented by inverting the data input to the second final stage of the power amplifier.

[0035] Fig. 9 shows an alternative embodiment of a bridge amplifier of the invention with a phase shift bridge output architecture, which is relatively more complex than that of Fig. 8, though capable of providing for enhanced performances, as described and illustrated in the above cited prior European patent application No. 98830685.8.

[0036] Fig. 10 shows a further embodiment of a bridge amplifier of the invention in which rather than inverting the data fed to the input of one of the pair of final power stages functioning in phase opposition, the inversion is implemented by inverting the up-down command of the respective counters of the second pair of PCM/PWM converters, such to generate triangular reference signals in phase opposition with each other.

[0037] A fourth embodiment of the bridge amplifier of the invention is illustrated in Fig. 11. According to this embodiment, the PWM signals of double frequency compared to the frequency of the main PWM signal relative to the conversion of the least significant bits are summed to the respective main PWM signals produced by the respective PCM/PWM converters fed with the most significant bits on the respective inverting input nodes of the two final power stages.

[0038] Another characteristic of the correction operated by the separate conversion of the least significant bits is a greater freedom because the correction current may be summed, subtracted or may not influence the main drive current signal relative to the conversion of most significant bits.

[0039] An advantage of a bridge embodiment of the amplifier of the invention is that the correction signal does not contain tones at the PWM switching frequency nor at frequencies near the switching frequency. Notably, tones in a ± 20 kHz band centered on the switching frequency are brought back in base band, causing an increase of the distortion and/or of noise.

[0040] In all the embodiments shown in the figures, is indicated the use of simple resistors for coupling PWM signals to the inverting input of the final power stage or stages (RMSB, RLSB, ...); however, as it will be evident to the skilled person these coupling resistors may be substituted by current generators driven by the logic signal output by the respective PCM/PWM converters.

Claims

1. A digital input PWM power amplifier comprising:

   an oversampling and noise shaping circuit receiving pulse code modulated (PCM) digital input data organized in words of a first number M of bits at a certain bit rate (Fin) and outputting pulse code modulated digital data organized in

words of a smaller number N of bits at a multiple bit rate (Fin*K);
a first bus transmitting a first number (P) of most significant bits (MSB) of said N bit words output from said first circuit and a second bus transmitting a second number (S) of least significant bits of said N bit words output from said first circuit;
first and second PCM/PWM converters, respectively fed with said first and second number of bits transmitted through said first and said second bus, each converter including a counter driven by a clock signal (Fclock) of frequency equal to the product of the bit rate (Fin*K) of the MSB and LSB bits transmitted on the respective bus and the square of the respective number of bits (P, S) generating reference digital words composed of said respective number of bits (P, S), defining ramps of digital values with a frequency identical to said multiple bit rate (Fin K), and a digital comparator receiving through a first input said reference digital words and through a second input the respective first and second number of bits (MSB, LSB) and outputting a respective PWM signal (MSBdig, LSBdig);
the PWM signal (MSBig) output by said first converter, being summed to the so attenuated PWM signal (LSBdig) output by said second converter on the inverting input node (-) of said output power stage.

2. The PWM amplifier according to claim 1, characterized in that said first and second PCM/PWM converters are of the single ramp type.

3. The PWM amplifier according to claim 1, characterized in that said first and second PCM/PWM converters, are of the double ramp type, said counter being of the up/down type and generating reference digital words composed of said second number (S) of least significant bits in the form of a succession of rising and falling ramps of a halved frequency compared to said multiple bit rate (Fin*k).

4. The PWM amplifier according to any of the preceding claims characterized in that is single ended and employs a single output power stage.

5. A PWM bridge amplifier according to any of claims 1, 2 and 3, having a pair of identical output power stages functioning in phase opposition in which the inversion of the driving signal to the inverting input of one of the two power stages is realized by inverting the PWM signals output by said pair of PCM/PWM converters.

6. A PWM bridge amplifier according to any of the claims 1, 2 and 3, employing a pair of identical output power stages functioning in phase opposition and in which the inversion of the driving signal of one of the two power stages is realized by inverting each of said first and second buses and duplicating said pair of PCM/PWM converters.

7. A PWM bridge amplifier according to any of the claims 1, 2 and 3, employing a pair of identical output power stages functioning in phase opposition in which the inversion of the driving signal fed to the inverting input of one of the two power stages is realized by duplicating said pair of PCM/PWM converters, coupling the inputs of the two converters forming said duplicated second pair of PCM/PWM converters to said first and second bus without preventively inverting them but inverting instead the ramp inversion commands (Fup-down) of the two PCM/PWM converters of said duplicated pair.

8. The amplifier according to claim 7, characterized in that it also comprises means for inverting the PWM signals output by the PCM/PWM converters of said two pairs of converters that are fed with said least significant bits (LSBdig), second attenuating means (RLSB2+RLSB1-) of said inverted signals and means to respectively sum said inverted and attenuated signals on the inverting input node to the signals produced by the other PCM/PWM converter of the respective pair of converters.

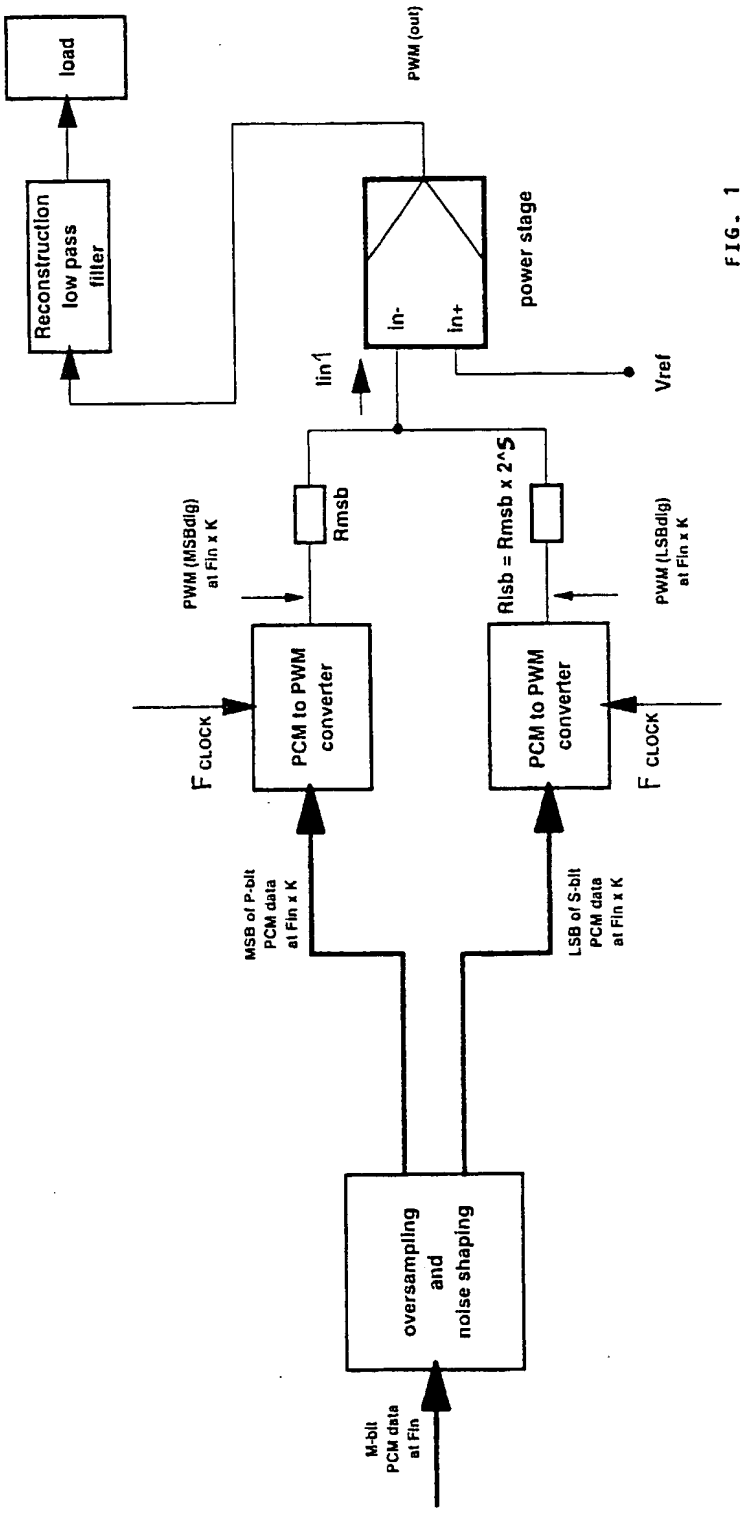
load
Reconstruction low pass filter
PWM (out)
power stage
in-
in+
Vref
Iin1
Rmsb
Rlsb = Rmsb x 2^5
PWM (MSBdig) at Fin x K
PWM (LSBdig) at Fin x K
PCM to PWM converter
PCM to PWM converter
F CLOCK
F CLOCK
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 1

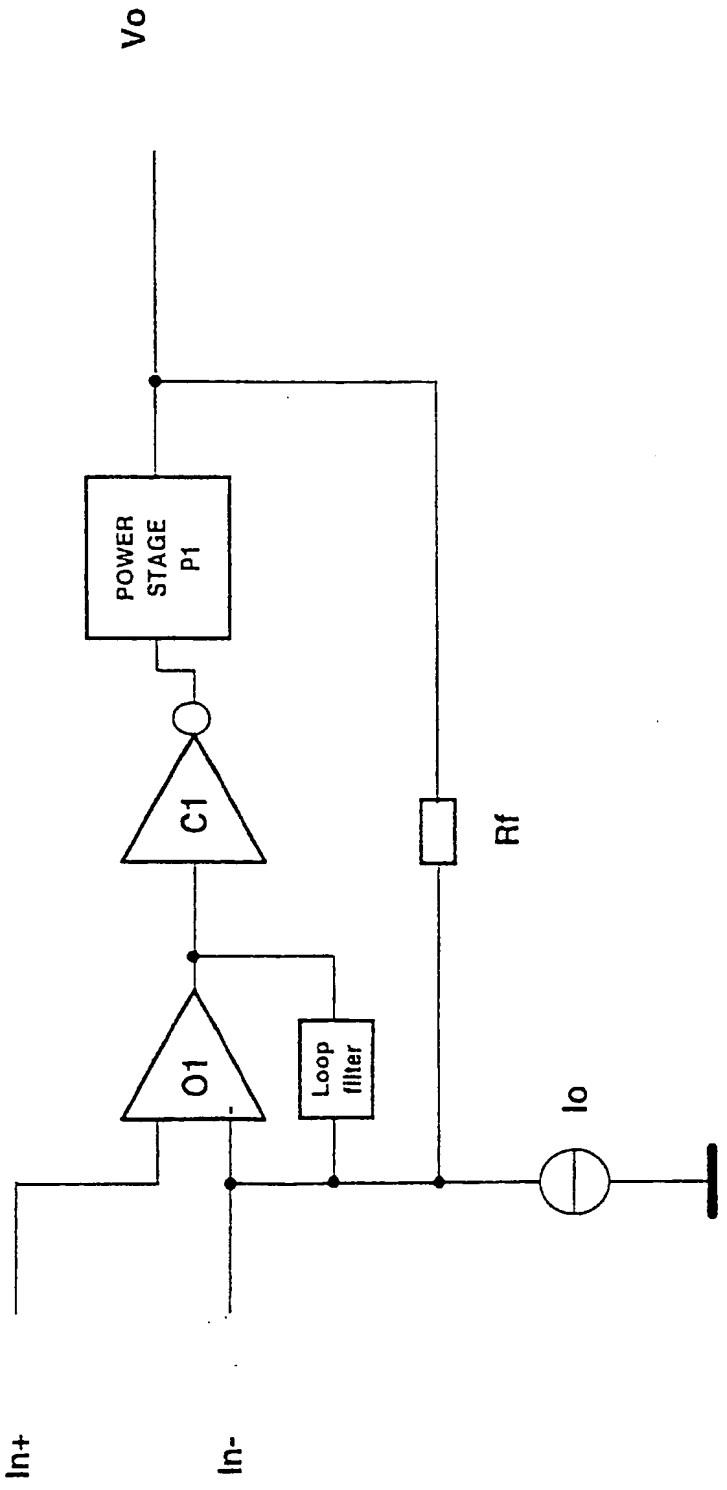

FIG. 2

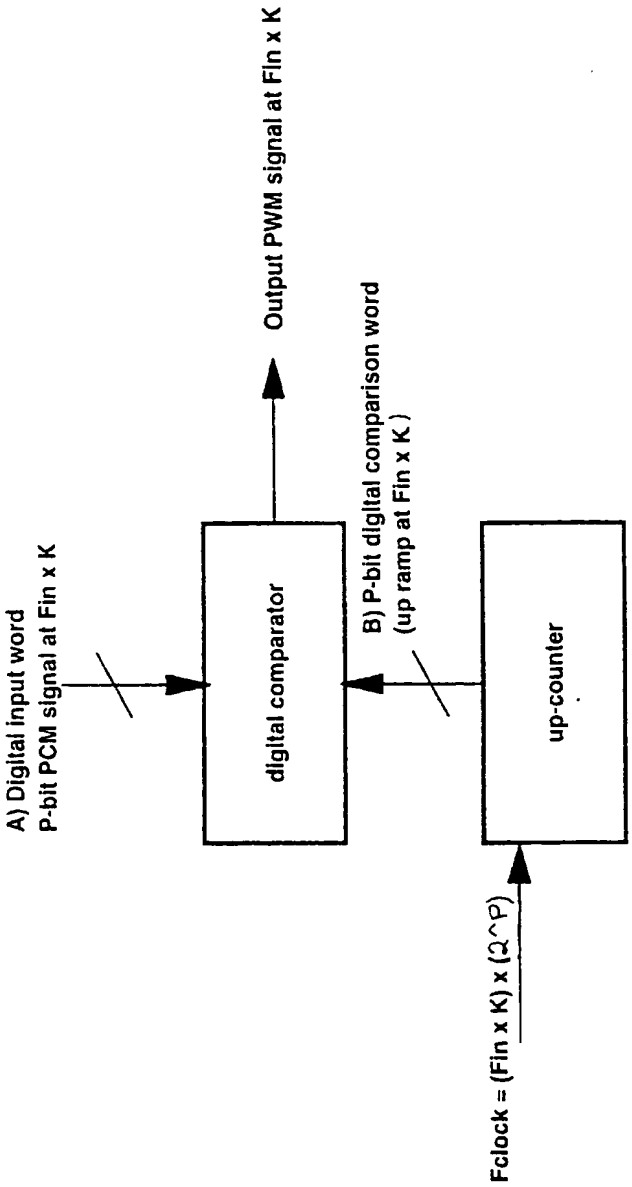
Output PWM signal at Fin x K
A) Digital input word
P-bit PCM signal at Fin x K
digital comparator
B) P-bit digital comparison word
(up ramp at Fin x K)
up-counter
Fclock = (Fin x K) x (2^P)

FIG. 3

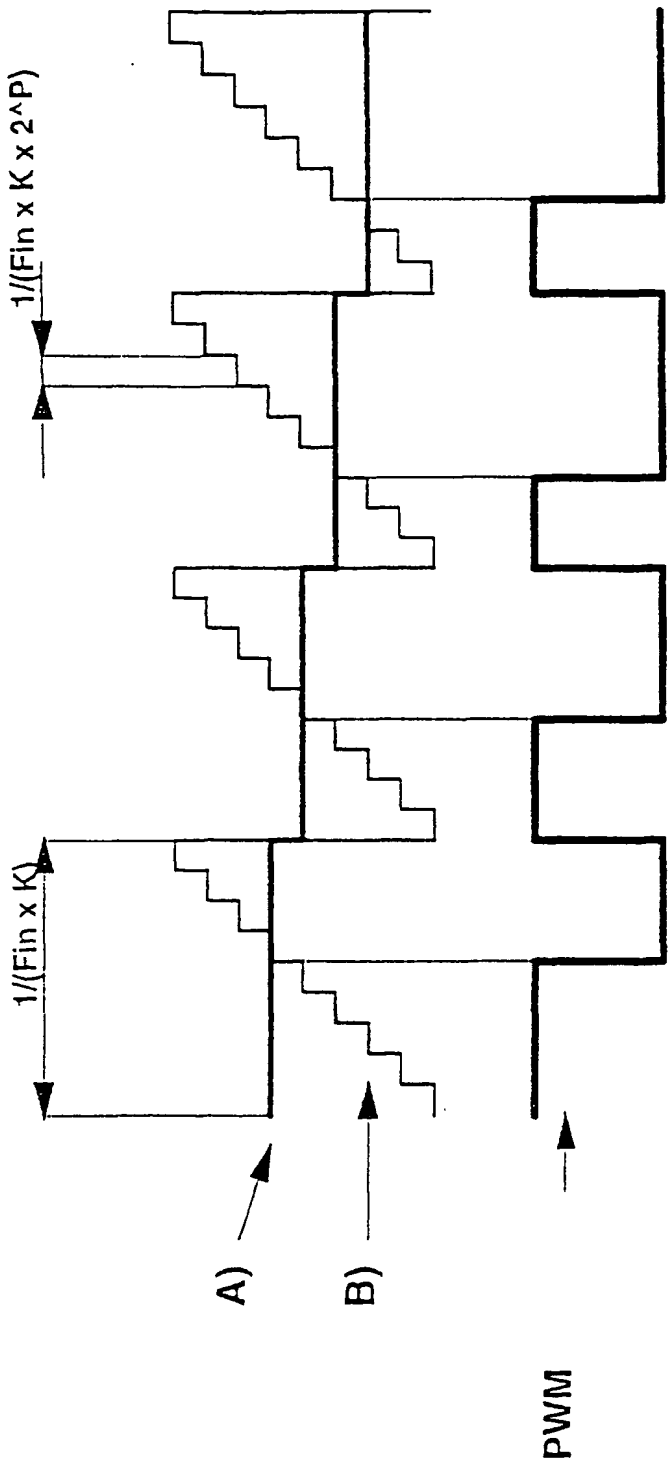

FIG. 4

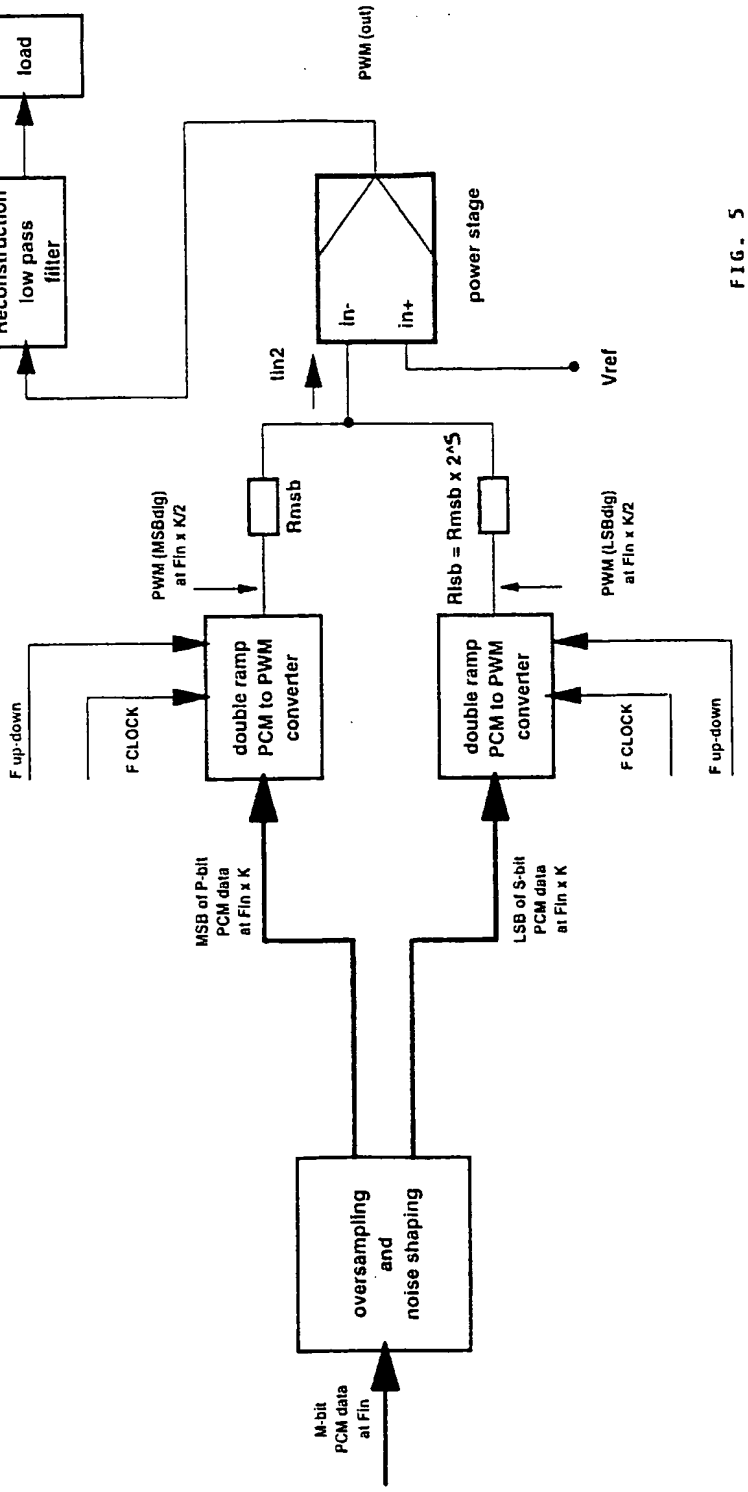
load
PWM (out)
Reconstruction low pass filter
power stage
in-
in+
Iin2
Vref
Rmsb
Rlsb = Rmsb x 2^5
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
double ramp PCM to PWM converter
double ramp PCM to PWM converter
F up-down
F CLOCK
F CLOCK
F up-down
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 5

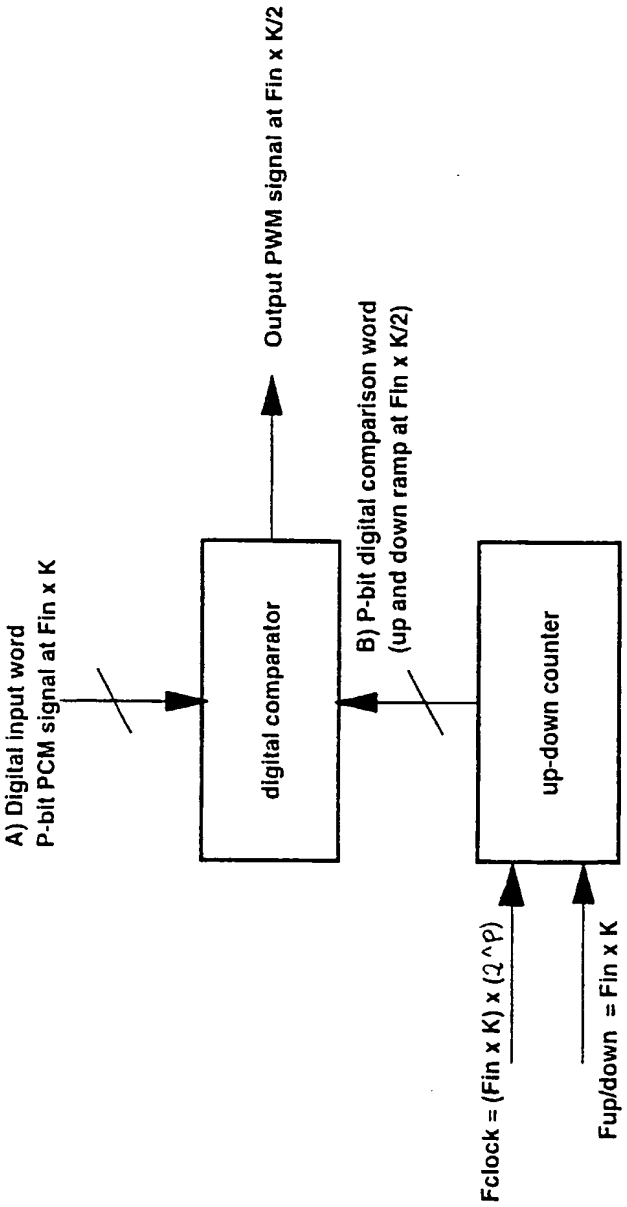
A) Digital input word
P-bit PCM signal at Fin x K
digital comparator
Output PWM signal at Fin x K/2
B) P-bit digital comparison word
(up and down ramp at Fin x K/2)
up-down counter
Fclock = (Fin x K) x (2^P)
Fup/down = Fin x K

FIG. 6

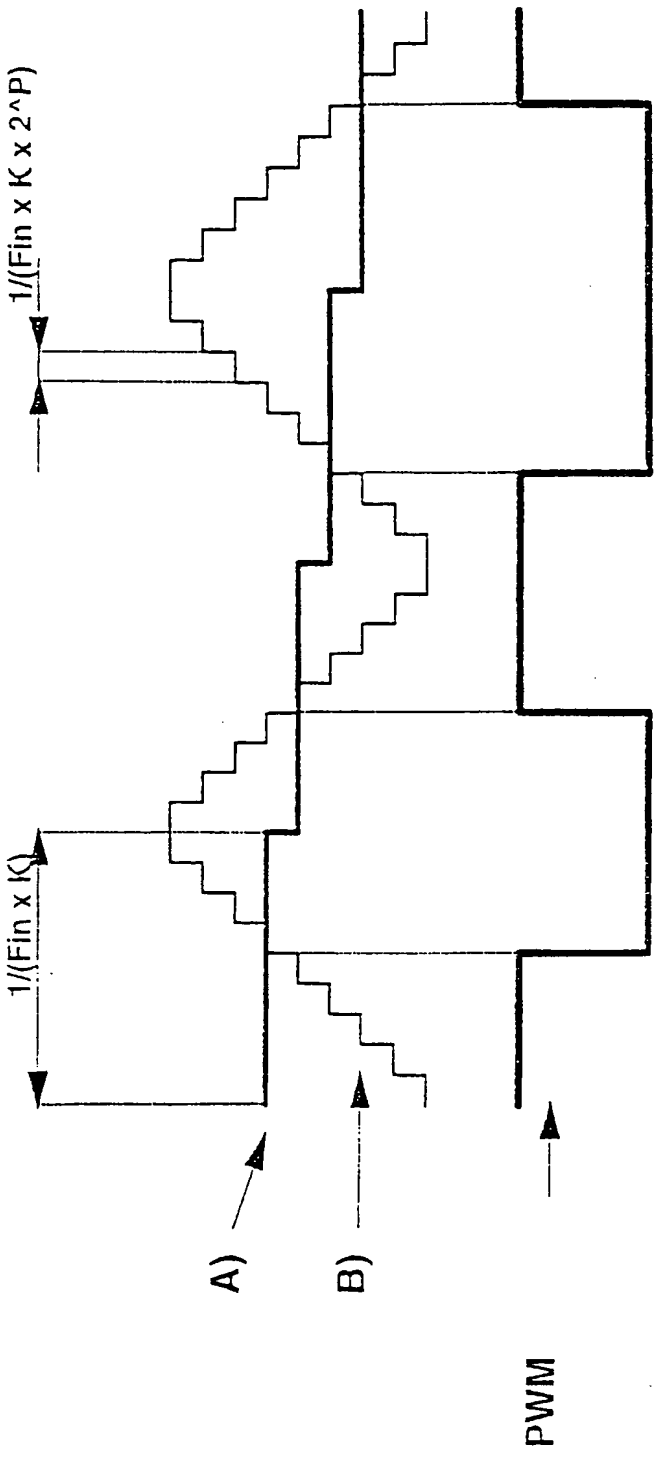

FIG. 7

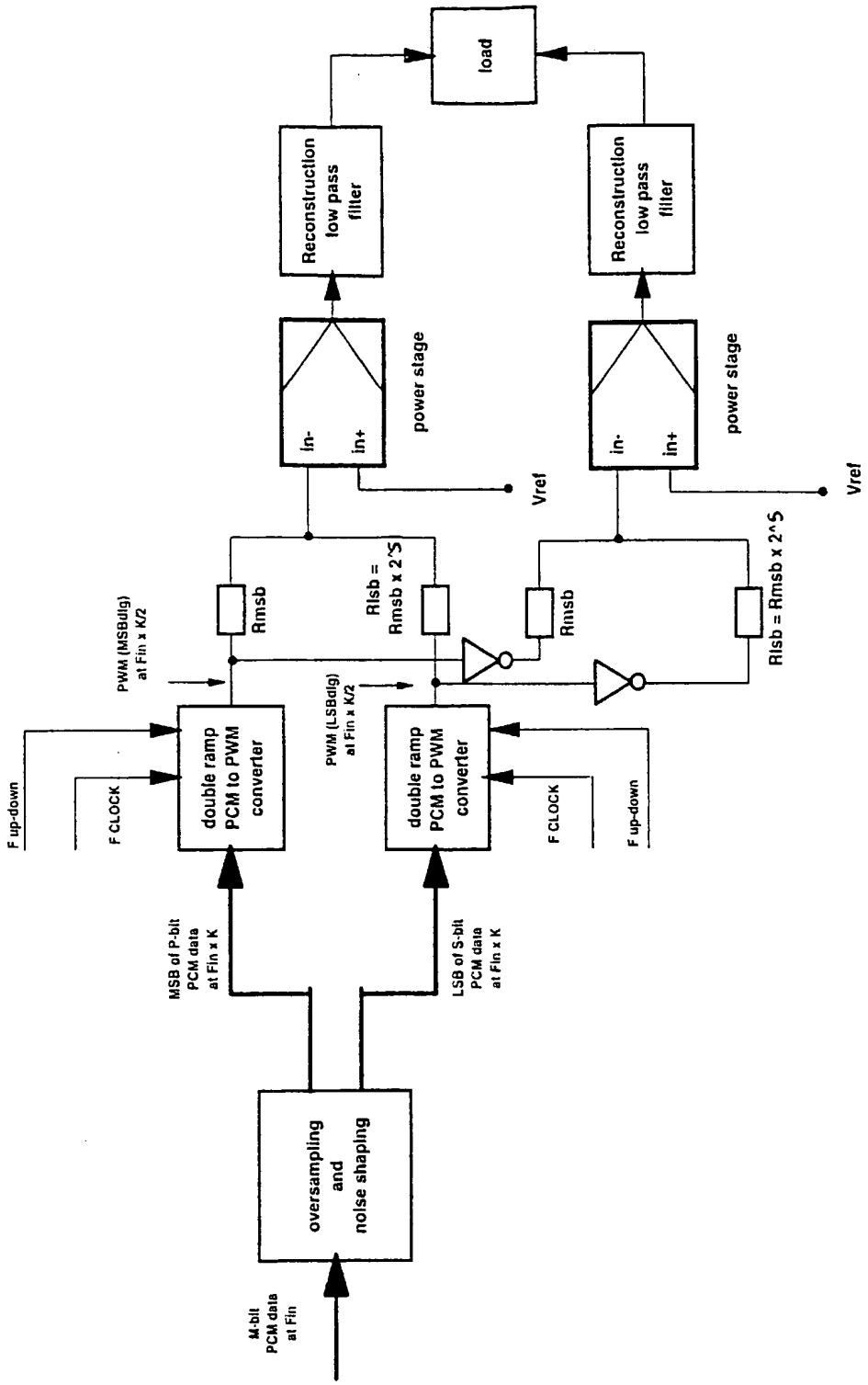
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
in-
in+
power stage
in-
in+
Vref
Vref
Rmsb
Rlsb = Rmsb x 2^S
Rmsb
Rlsb = Rmsb x 2^S
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
double ramp PCM to PWM converter
F CLOCK
F up-down
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 8

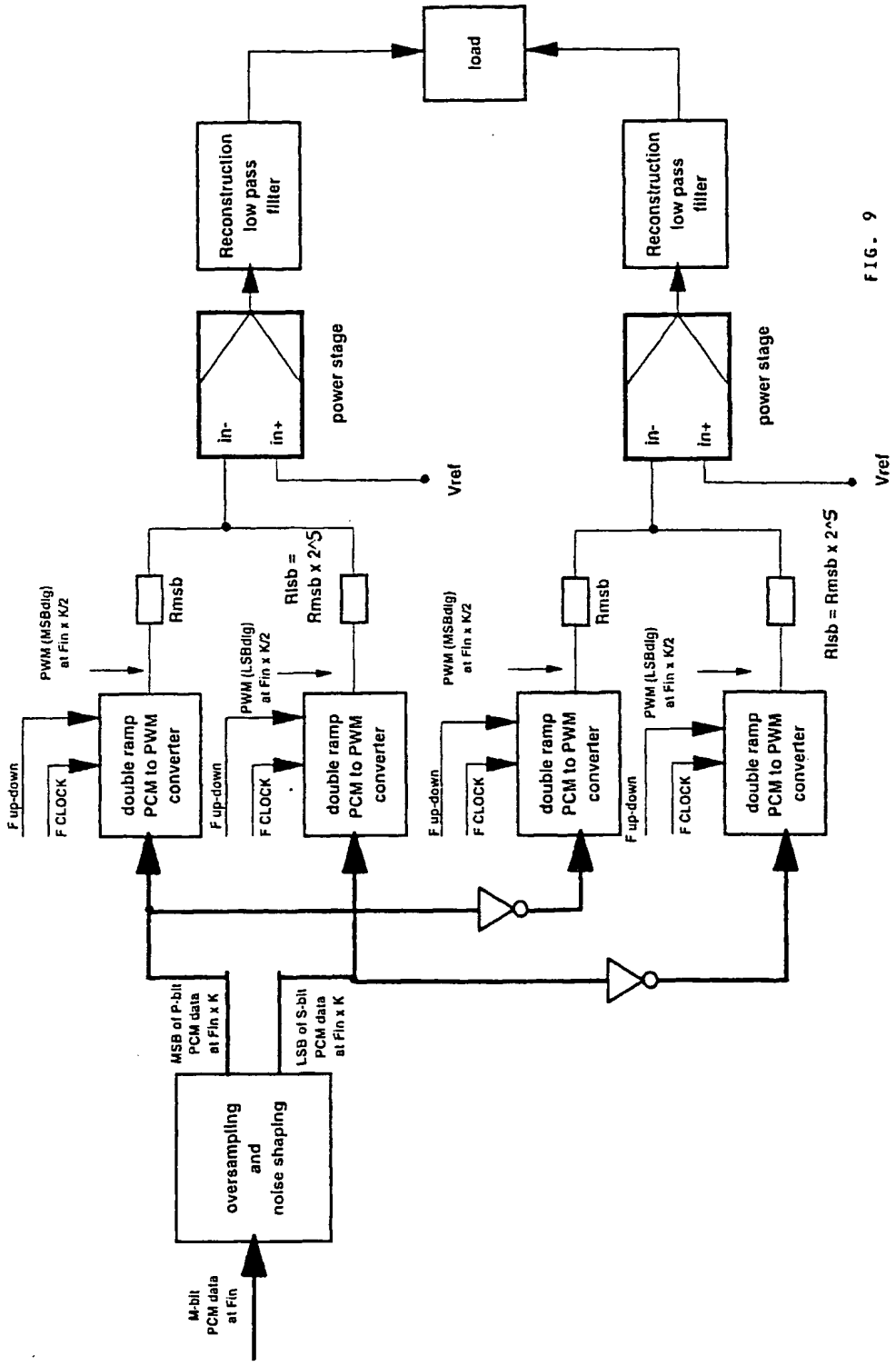
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
in-
in+
power stage
in-
in+
Vref
Vref
Rmsb
Rlsb = Rmsb x 2^5
Rmsb
Rlsb = Rmsb x 2^5
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
PWM (MSBdig) at Fin x K/2
PWM (LSBdig) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
F up-down
F CLOCK
double ramp PCM to PWM converter
F up-down
F CLOCK
double ramp PCM to PWM converter
F up-down
F CLOCK
double ramp PCM to PWM converter
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 9

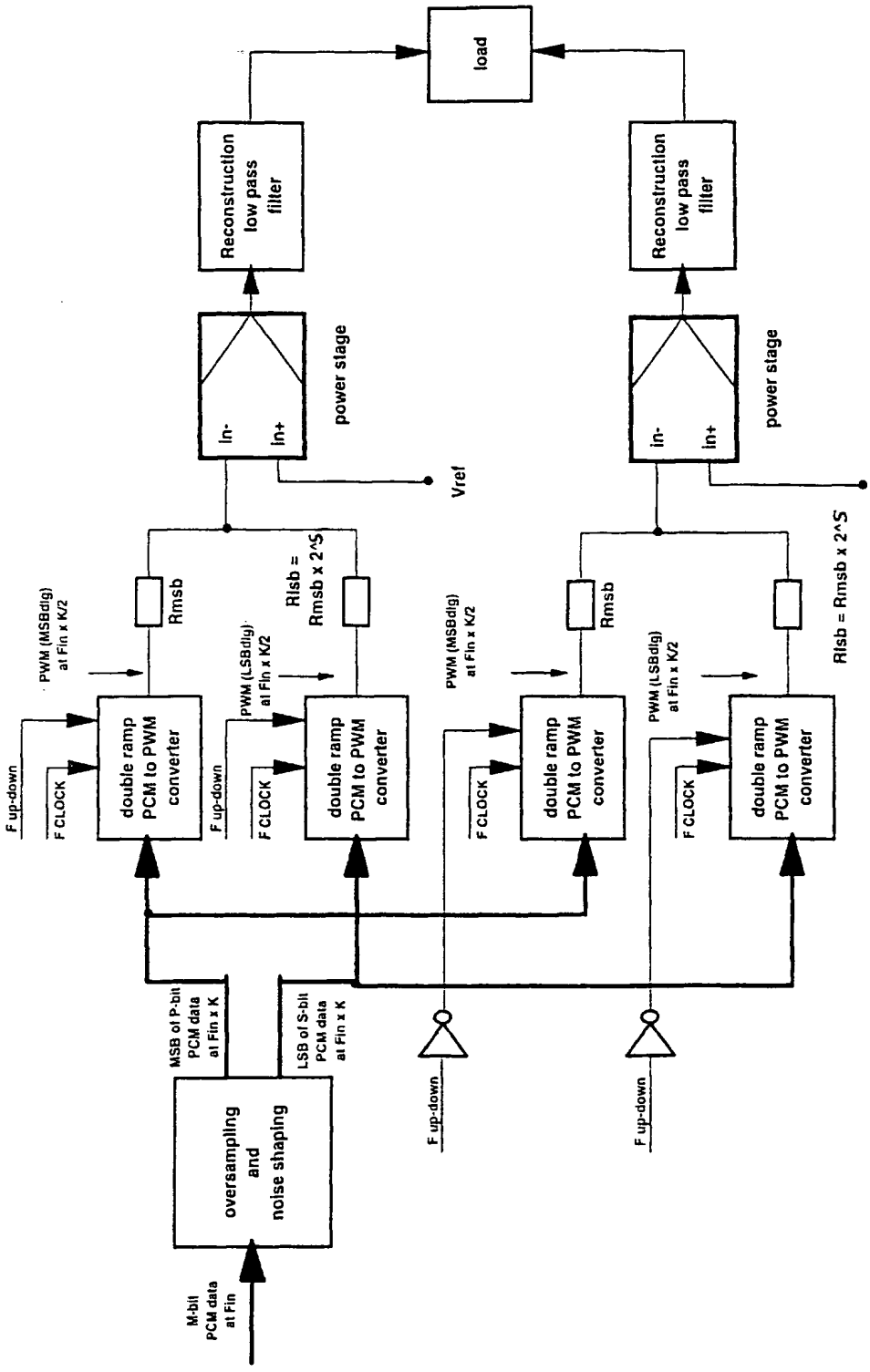
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
in-
in+
power stage
in-
in+
Vref
Vref
Rmsb
Rlsb = Rmsb x 2^S
Rmsb
Rlsb = Rmsb x 2^S
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
F up-down
F CLOCK
double ramp PCM to PWM converter
F CLOCK
double ramp PCM to PWM converter
F CLOCK
double ramp PCM to PWM converter
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
F up-down
F up-down
oversampling and noise shaping
M-bit PCM data at Fin

FIG. 10

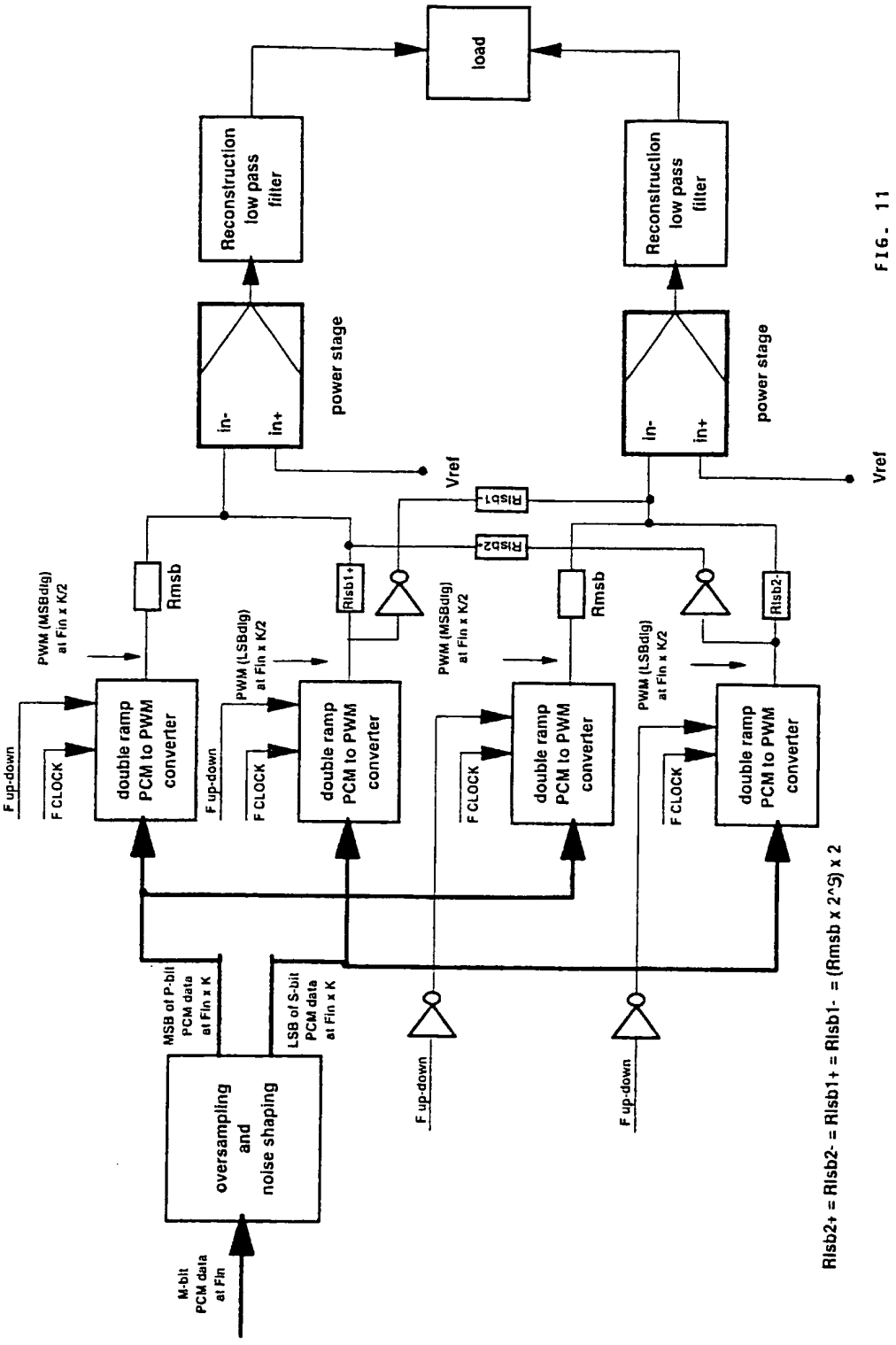
load
Reconstruction low pass filter
Reconstruction low pass filter
power stage
power stage
in-
in+
in-
in+
Vref
Vref
Rlsb1-
Rlsb2-
Rmsb
Rmsb
Rlsb1+
Rlsb2-
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
PWM (MSBdlg) at Fin x K/2
PWM (LSBdlg) at Fin x K/2
F up-down
F CLOCK
double ramp PCM to PWM converter
F up-down
F CLOCK
double ramp PCM to PWM converter
F CLOCK
double ramp PCM to PWM converter
F CLOCK
double ramp PCM to PWM converter
MSB of P-bit PCM data at Fin x K
LSB of S-bit PCM data at Fin x K
oversampling and noise shaping
M-bit PCM data at Fin
F up-down
F up-down
Rlsb2+ = Rlsb2- = Rlsb1+ = Rlsb1- = (Rmsb x 2^S) x 2

FIG. 11

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Application Number
EP 99 83 0073

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Place of search	Date of completion of the search	Examiner
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